CLAIMS

What is claimed is:

1. An integrated circuit having scan test features and including:

a scan test signal interceptor for intercepting scan test related signals applied to the integrated circuit; and

a security element responsive to the scan test signal interceptor to preclude retrieval of secure information within the integrated circuit using the scan test related signals.

2. The integrated circuit of claim 1 wherein the security element comprises:

a reset generator to reset secure information within the integrated circuit.

3. The integrated circuit of claim 2 wherein the scan test signal interceptor is operable to sense a request to enter scan test.

4. The integrated circuit of claim 3 wherein the reset generator is operable to reset secure information in response the request to enter scan test.

5. The integrated circuit of claim 2 wherein the scan test signal interceptor is operable to sense a request to exit scan test.

6. The integrated circuit of claim 5 wherein the reset generator is operable to reset secure information in response the request to exit scan test.

7. A method operable within an integrated circuit to prevent unauthorized access to secure information, the method comprising:

detecting application of a scan test related signal to the integrated circuit; and

precluding access to the secure information in response to detection of the scan test related signal.

8. The method of claim 7 wherein the step of precluding includes:

resetting elements of the integrated circuit to reset the secure information.

9. The method of claim 7 wherein the step of detecting includes:

detecting a signal applied to the integrated circuit requesting entry to scan test.

10. The method of claim 9 wherein the step of resetting includes:

resetting elements of the integrated circuit in response to detection of the request to enter scan test.

11. The method of claim 9 wherein the step of detecting includes:

detecting a signal applied to the integrated circuit requesting exit from scan test.

12. The method of claim 11 wherein the step of resetting includes:

resetting elements of the integrated circuit in response to detection of the request to exit scan test.

13. A system including an integrated circuit having a scan test capability, the system comprising:

means for detecting scan test operation of the integrated circuit; and

means for precluding retrieval of secure information within the integrated circuit in response to detecting scan test operation.

14. The system of claim 13 wherein the means for precluding includes:

reset means for resetting the secure information within the integrated circuit to preclude retrieval thereof using scan test operation.

15. The system of claim 14 wherein the reset means is operable to generate a reset within the integrated circuit in response to sensing entry to scan test of the integrated circuit.

16. The system of claim 14 wherein the reset means is operable to generate a reset within the integrated circuit in response to sensing exit from scan test of the integrated circuit.